REMARKS

First note regarding claims

Applicant respectfully requests that the Examiner reconsider his rejections made in the final office action. Applicant believes that the claims as previously presented are allowable, and is prepared to appeal the present patent application to the Board of Patent Appeals and Interference. However, Applicant would prefer to avoid having to appeal this patent application to save both Applicant and the Examiner time. Therefore, the Examiner is respectfully requested to contact Applicant's Attorney, Mike Dryja, at the phone number listed below, with any proposed claim amendments that if made would render the present application in condition for allowance. That is, if the Examiner were to propose to Applicant claim amendments that would render the present application in condition for formal allowance without the need for filing an appeal or a request for continuing examination (RCE), Applicant would more than likely accept such claim amendments to secure allowance.

Second note regarding claims

In the previous office action response of November 3, 2008, Applicant cancelled claims 1-8 and 17 without prejudice. It is noted that the Examiner examined claims 1-8 and 17-21 in the office action of August 4, 2008.

In the present final office action response, Applicant has reintroduced claims 1-8 and 17 in the same state as they were when examined by the Examiner in the office action of August 4, 2008; that is, claims 1-8 and 17 have not been amended subsequent to their examination in the office action of August 4, 2008.

Applicant therefore submits that claims 1-8 and 17 are properly reintroduced in the present final office action response, as the Examiner does not have to perform any further search or consideration of these claims (i.e., a search has already been performed, and the Examiner has

already examined these claims). Applicant apologizes for the confusion of first cancelling these claims and then reintroduces them. Nevertheless, Applicant respectfully requests that the Examiner formally indicate in the next action (such as an advisory action) that claims 1-8 and 17 have been reentered in this patent application.

Claim rejections under 35 USC 102

Claims 9-11 and 15 have been rejected under 35 USC 102(b) as being anticipated by Irie (6,038,644). Claims 9 and 15 are independent claims, and claims 10-11 depend from claim 9. Applicant respectfully submits that as previously presented, claims 9 and 15 are patentable over Irie, such that claims 10-11 are patentable at least because they depend from a patentable base independent claim.

Applicant respectfully requests that the Examiner reconsider his rejection of claims 9 and 15. In the previous office action response, Applicant explained how the claimed invention selectively broadcasts a *cache miss* to a sub-plurality of nodes, whereas Irie selectively broadcasts a *coherent processing request* to a sub-plurality of nodes. The Examiner has stated that Applicant's argument is misleading (final office action, p. 7, para. 6). Applicant disagrees. The Examiner goes on to state that "Irie clearly teaches to generate a coherent processing request in response to cache miss notification" (id.), which Applicant agrees with, and that "the coherent processing request clearly includes cache miss, thereby the coherent request as used in Irie is considered as a cache miss" (id.,), which Applicant disagrees with.

Rather, it is clear in Irie that a coherent processing request is clearly *not* a cache miss. Irie says that there is a miss in cache memory, which is detected, and in response, a coherent processing request is generated.[1] If the cache miss were the same as the coherent processing

[1] Irie explicitly says the following:

> When the miss of the cache memory 300 is detected by the hit detect logic 352 in the cache control unit 350 (FIG. 3), the judge result of the hit check is notified [sic] to the cache status control logic 354 through line 3520. *The cache*

request in Irie, then there would be no need to then generate a coherent processing request in Irie. That is, in Irie, there is a cache miss, and a coherent processing request. Applicant does not deny that the coherent processing request is related to the cache miss, in that the former is generated in response to the latter. However, it cannot be said that the coherent processing request can be considered as the cache miss, because if the request were considered the cache miss, then there would be no point in generating the coherent processing request in response to detecting the cache miss.

Indeed, the definition of a cache miss and the definition of a coherent processing request are very much different. Irie states that the "coherent processing request requests the other processor units to execute processing for maintenance of coherency concerning the data of the address designated by the previously executed memory access instruction" (col. 7, ll. 53-66). Irie does not explicitly define what a cache miss is, but the Internet web site en.wikipedia.org/wiki/CPU_cache#Cache_misses relevantly defines a cache miss as follows: "A cache miss refers to a failed attempt to read or write a piece of data in the cache, which results in a main memory access with much longer latency." It is noted that this definition is consistent with the usage of the term cache miss as used in Irie (see, e.g., col. 5, ll. 27-41).

Therefore, Applicant respectfully submits that a coherent processing request clearly does *not* include a cache miss, in contradistinction to the Examiner's assertion to the contrary. The

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> *status control logic 354 responds to this notification, and generates a coherent processing request* in the register 360 (FIG. 4). . . . The coherent processing request requests the other processor units to execute processing for maintenance of coherency concerning the data of the address designated by the previously executed memory access instruction.
>
> . . . .
>
> When a coherent processing request is transferred to other plural processor units, the present embodiment controls its destination so that it does not transfer the request to all other processor units but only to part of the processor units which are likely to have cached the data designated by the request.

(Col. 7, ll. 44-56; col. 8, ll. 17-21).

coherent processing request is very much different than a cache miss. A cache miss is a failed attempt to read or write data in a cache. A coherent processing request requests that other processing units execute processing to maintain coherency of data. A cache miss is just that, in other words – a statement of objective fact that an attempt to access data in a cache has failed, or has "missed." By comparison, a coherent processing request is just that, a request to perform coherent processing. A request to perform some type of processing is not the same as a statement of objective fact; thus, a request to perform coherent processing is not the same as a cache miss.

The Examiner has stated that a coherent processing request "clearly includes" a cache miss (final office action p. 7, para. 6). However, Applicant respectfully submits that the Examiner's statement misconstrues what Irie actually says. Irie says that in response to detecting a cache miss, a coherent processing request is generated. Therefore, Irie "clearly" generates a coherent processing request in response to detecting a cache miss. What Irie does not "clearly" state – either inherently or explicitly – is that a coherent processing request "includes" a cache miss: the Examiner has not explained how a coherent processing request "clearly" includes a cache miss, in contradiction to his *prima facie* obligation to do so. At the end of the day, a coherent processing request is simply just not a cache miss, as has been explained above; just because it is generated in response to detecting a cache miss does not mean that such a coherent processing request "includes" the cache miss, in contradistinction to the Examiner's assertion to the contrary without explanation.

Ultimately, then, the claimed invention can be distinguished from Irie diagrammatically as follows. The claimed invention selectively broadcasts a cache miss CM to a sub-plurality of nodes N. Irie detects a cache miss CM, and in response generates and a coherent processing request CPR and selectively broadcasts this coherent processing request CPR to a sub-plurality of nodes N. Thus, in the claimed invention:

CM → N

By comparison, in Irie:

Detect CM
In response,
Generate CPR
CPR → N

As such, it is very clear that Irie does not identically disclose the claimed invention, and that there is a difference between that which Irie discloses and that which the invention claims.[2]

Finally, the Examiner has stated that "the claimed language fails to explicitly define how to broadcast [a] cache miss," such that "the broad claimed language can be read by Irie" (Final office action, p. 7, para. 6). The Examiner's acknowledgment that the claim language does not define how a cache miss is broadcast, however, is a red herring, and is besides the point. The claim language *does* explicitly recite that it is a *cache miss* that is selectively broadcast. By comparison, Irie does *not* selectively broadcast a cache miss, but rather selectively broadcasts a request that is generated *in response to generating a cache miss*. Therefore, Irie cannot be said to anticipate the invention, because the "thing" that it selectively broadcasts – a coherent processing request – is not a cache miss, and does not inherently or explicitly include a cache miss.

[2] Applicant notes in this respect that the standard for anticipation under 35 USC 102 is that every aspect of a claim must *identically* appear in a single prior art reference for it to anticipate the claim under 35 USC 102. (In re Bond, 15 USPQ2d 1566 (Fed. Cir. 1990)) "[T]here must be *no difference* between the claimed invention and the reference disclosure, as viewed by a person of ordinary skill in the field of the invention." (Scripps Clinic & Research Found. v. Genentech, Inc., 18 USPQ2d 1001, 1010 (Fed. Cir. 1991))

Claim rejections under 35 USC 103

Claims 12-14 and 16 have been rejected under 35 USC 103(a) as being unpatentable over Irie in view of Steely (2005/0160430). Claims 12-14 are dependent claims depending from claim 9, and therefore are patentable at least because claim 9 is patentable, as discussed above. Claim 16 is an independent claim, and includes the same limitations that have been discussed above in relation to independent claims 9 and 15. Therefore, claim 16 is patentable over Irie in view of Steely for at least substantially the same reasons that claims 9 and 15 are patentable over Irie alone, as has been discussed above.

Represented claims 1-8 and 17

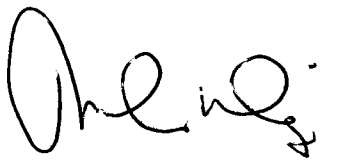
Claims 1 and 17 are independent claims, and claims 2-8 depend from claim 1. Claims 1-2 and 17 were previously rejected by the Examiner as being anticipated by Irie. Claims 1 and 17 include the same limitations that have been discussed above in relation to independent claims 9 and 15. Therefore, claims 1 and 17 are patentable over Irie for at least substantially the same reasons that claims 9 and 15 are patentable over Irie alone, as has been discussed above.

Claims 3-8 were previously rejected by the Examiner as being unpatentable over Irie in view of Steely. Claims 3-8 depend from claim 1. Therefore, claims 3-8 are patentable at least because they depend from a patentable base independent claim, claim 1.

Conclusion

Applicants have made a diligent effort to place the pending claims in condition for allowance, and request that they so be allowed. However, should there remain unresolved issues that require adverse action, it is respectfully requested that the Examiner telephone Mike Dryja, Applicant's representative, at 425-427-5094, so that such issues may be resolved as expeditiously as possible; Applicant is amenable to proposals from the Examiner that would render the claims allowable without having to resort to appeal. For the reasons discussed above, this application is now considered to be in condition for allowance and such action is earnestly solicited.

Respectfully Submitted,



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